ABSTRACT OF THE DISCLOSURE

A memory device (**200**) can include memory cell arrays (**202**-a and **202**-b) accessed according to phase shifted clock signals. Memory cell array (**202**-a) can be accessed at double data rates essentially synchronous with clock signal CLK. Memory cell array (**202**-b) can be accessed at double data rates essentially synchronous with a phase delayed clock signal DCLK. Such an arrangement can provide eight data accesses (four reads and four writes) in a single clock cycle.